

May 1988 Revised October 2000

74F379

Quad Parallel Register with Enable

General Description

The 74F379 is a 4-bit register with buffered common Enable. This device is similar to the 74F175 but features the common Enable rather than common Master Reset.

Features

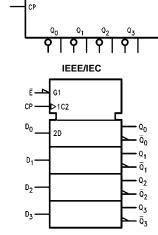
- Edge triggered D-type inputs
- Buffered positive edge-triggered clock
- Buffered common enable input
- True and complement outputs

Ordering Code:

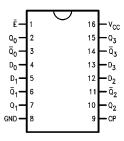
Order Number	Package Number	Package Description
74F379SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F379SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F379PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Danasiutia u	U.L.	Input I _{IH} /I _{IL}	
Pin Names	Description	HIGH/LOW	Output I _{OH} /I _{OL}	
Ē	Enable Input (Active LOW)	1.0/1.0	20 μA/–0.6 mA	
D ₀ -D ₃	Data Inputs	1.0/1.0	20 μA/–0.6 mA	
СР	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/–0.6 mA	
Q_0 – Q_3	Flip-Flop Outputs	50/33.3	−1 mA/20 mA	
$\overline{Q}_0 - \overline{Q}_3$	Complement Outputs	50/33.3	−1 mA/20 mA	

Functional Description

The 74F379 consists of four edge-triggered D-type flipflops with individual D inputs and Q and \overline{Q} outputs. The Clock (CP) and Enable (\overline{E}) inputs are common to all flipflops. When the \overline{E} is input HIGH, the register will retain the present data independent of the CP input. The D_{n} and $\overline{\boldsymbol{E}}$ inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

Truth Table

		Inputs	Out	puts	
i	Ē	СР	D_n	Q_n	$\overline{\mathbf{Q}}_{\mathbf{n}}$
I	+		Х	NC	NC
	L	~	Н	Н	L
	L	~	L	L	Н

H = HIGH Voltage Level

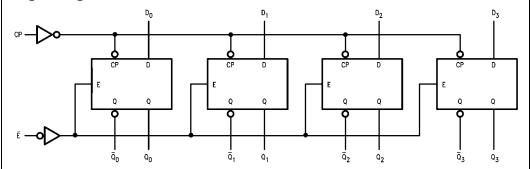
L = LOW Voltage Level

X = Immaterial

= LOW-to-HIGH Transition

NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

+4.5V to +5.5V

Absolute Maximum Ratings(Note 1)

-65°C to +150°C

Storage Temperature Ambient Temperature under Bias -55°C to +125°C

Junction Temperature under Bias $-55^{\circ}C$ to $+150^{\circ}C$ V_{CC} Pin Potential to Ground Pin -0.5V to +7.0V

Input Voltage (Note 2) -0.5V to +7.0V Input Current (Note 2) -30~mA to +5.0~mA

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

Standard Output -0.5V to V_{CC} 3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA) ESD Last Passing Voltage (Min)

Conditions Free Air Ambient Temperature 0°C to +70°C

Recommended Operating

Supply Voltage

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

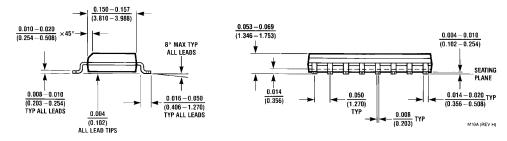
Symbol	nbol Parameter		Parameter Min Typ Max Units		v _{cc}	Conditions		
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH	10% V _{CC}	2.5			V	Min	I _{OH} = -1 mA
	Voltage	$5\% V_{CC}$	2.7			V	IVIIII	$I_{OH} = -1 \text{ mA}$
V _{OL}	Output LOW	10% V _{CC}			0.5	V	Min	1 - 20 mA
	Voltage				0.5	V	IVIIII	I _{OL} = 20 mA
I _{IH}	Input HIGH				5.0	μА	Max	V _{IN} = 2.7V
	Current				3.0	μΛ	IVIAX	V IN - 2.7 V
I _{BVI}	Input HIGH Current				7.0	μА	Max	V _{IN} = 7.0V
	Breakdown Test				7.0	μΛ	IVIAX	V _{IN} = 7.0V
I _{CEX}	Output HIGH				50	^	Max	V _{OUT} = V _{CC}
	Leakage Current				50	μА	IVIAX	VOUT = VCC
V _{ID}	Input Leakage		4.75			V	0.0	$I_{ID} = 1.9 \mu A$
	Test		4.75			V	0.0	All Other Pins Grounded
I _{OD}	Output Leakage				3.75	μА	0.0	V _{IOD} = 150 mV
	Circuit Current				3.73	μΑ	0.0	All Other Pins Grounded
I _{IL}	Input LOW Current				-0.6	mA	Max	V _{IN} = 0.5V
los	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V
I _{CCL}	Power Supply Current			28	40	mA	Max	$V_0 = LOW$

AC Electrical Characteristics

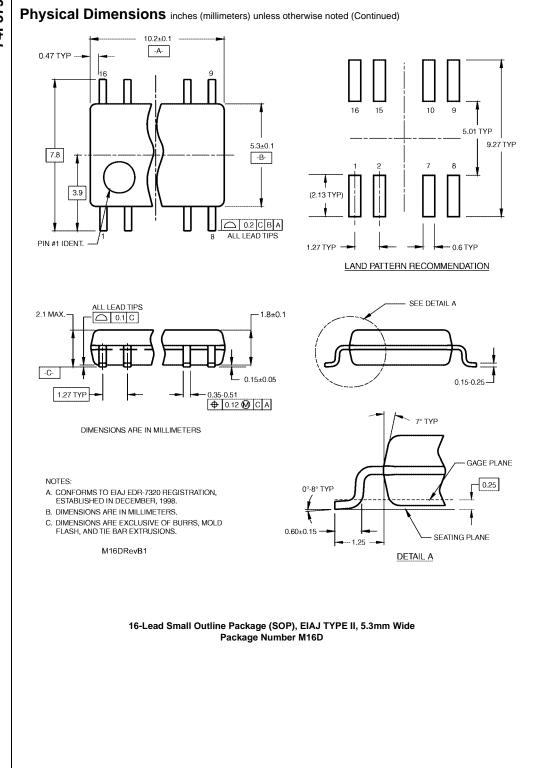
Symbol	Parameter	$T_{A} = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_{L} = 50 \text{ pF}$			$T_A = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		Units
		Min	Тур	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	100	140		75		100		MHz
t _{PLH}	Propagation Delay	3.5	5.0	6.5	3.0	8.5	3.5	7.5	ns
t _{PHL}	CP to Q_n , \overline{Q}_n	5.0	6.5	8.5	4.0	10.0	5.0	9.5	115

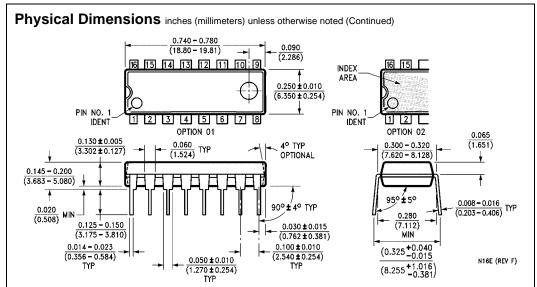
AC Operating Requirements

Symbol	Parameter	1	T _A = +25°C V _{CC} = +5.0V Min Max		$T_{A} = -55^{\circ}C \text{ to } +125^{\circ}C$ $V_{CC} = +5.0V$ $Min \qquad Max$		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ Min Max	
Зушьог	raianietei							
t _S (H)	Setup Time, HIGH or LOW	3.0		4.0			3.0	
t _S (L)	D _n to CP	3.0		4.0			3.0	
t _H (H)	Hold Time, HIGH or LOW	1.0		2.0			1.0	ns
$t_H(L)$	D _n to CP	1.0		2.0			1.0	
t _S (H)	Setup Time, HIGH or LOW	6.0		8.0			6.0	
$t_S(L)$	E to CP	6.0		8.0			6.0	ns
t _H (H)	Hold Time, HIGH or LOW	0		0			0	115
$t_H(L)$	E to CP	0		0			0	
t _W (H)	CP Pulse Width	4.0		5.0			4.0	ns
$t_W(L)$	HIGH or LOW	5.0		7.0			5.0	115



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A





16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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